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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,131	06/01/2006	Shuji Hagino	JP 030022	2663
24737 7590 06/23/2009 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510				
EXAMINER				
ZUBAJLO, JENNIFER L				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/596,131

Applicant(s)

HAGINO ET AL.

Examiner

JENNIFER ZUBAJLO

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 June 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-893)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terence R. Klein (Pub. No.: US 2003/0193458).

As to claim 1, Klein teaches a driving circuit for driving a capacitive load of a display device, comprising: driving signal supplying means for supplying a driving signal having a target voltage to be applied (see [0001]); an amplifying stage for receiving the driving signal and selectively outputting the driving signal to the capacitive load (see fig. 4 – amplifier 450); and a pair of current sources for selectively supplying a positive current and a negative current to the capacitive load, respectively during their on-states, the driving circuit repeating a repetitive operation including a pre-operation where any one of the current sources is switched ON in accordance with the driving signal and then switched OFF and a post-operation where the amplifying stage is switched to a state for outputting the driving signal to the capacitive load after the pre-operation (see fig. 4 – current sources 420 & 430 – note that it is obvious for the currents to be positive or negative depending on the DAC).

As to claim 2, Klein teaches a driving circuit according to claim 1 (see above rejection), wherein a duration length of an ON period of the relevant current source and/or a current supply rate of the relevant current source during the pre-operation is made variable in accordance with a value of the driving signal in a repetition period of the repetitive operation (see [0050] and fig. 7).

As to claim 3, Klein teaches a driving circuit according to claim 1 (see above rejection), wherein a duration length of an ON period of the relevant current source and/or a current supply rate of the relevant current source during the pre-operation is made variable in accordance with a value of the driving signal in a repetition period of the repetitive operation and a value of the driving signal in another repetition period previous to said repetition period (see [0050] and fig. 7).

As to claim 7, Klein teaches a driving circuit according to claim 1 (see above rejection), wherein the target voltage is a gray-scale voltage (see [0033]).

As to claim 8, Klein teaches a driving circuit according to claim 1 (see above rejection), wherein the capacitive load is a liquid crystal cell (see [0001]).

As to claim 9, Klein teaches a driving circuit according to claim 1 (see above rejection), wherein the driving signal supplying means includes analog to digital converting means (see fig. 4).

As to claim 10, Klein teaches a display device using a driving circuit according to claim 1 (see fig. 1).

3. Claims 1-3 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hitoshi Tsuge (Pub. No.: US 2007/0132674).

As to claim 1, Tsuge teaches a driving circuit for driving a capacitive load of a display device, comprising: driving signal supplying means for supplying a driving signal having a target voltage to be applied (see [0001]); an amplifying stage for receiving the driving signal and selectively outputting the driving signal to the capacitive load (see [0570]); and a pair of current sources for selectively supplying a positive current and a negative current to the capacitive load, respectively during their on-states, the driving circuit repeating a repetitive operation including a pre-operation where any one of the current sources is switched ON in accordance with the driving signal and then switched OFF and a post-operation where the amplifying stage is switched to a state for outputting the driving signal to the capacitive load after the pre-operation (see fig. 113 – current sources 1112 and 1113 - note that it is obvious for the currents to be positive or negative depending on gray level).

As to claim 2, Tsuge teaches a driving circuit according to claim 1 (see above rejection), wherein a duration length of an ON period of the relevant current source and/or a current supply rate of the relevant current source during the pre-operation is made variable in accordance with a value of the driving signal in a repetition period of the repetitive operation (see fig. 114).

As to claim 3, Tsuge teaches a driving circuit according to claim 1 (see above rejection), wherein a duration length of an ON period of the relevant current source and/or a current supply rate of the relevant current source during the pre-operation is made variable in accordance with a value of the driving signal in a repetition period of the repetitive operation and a value of the driving signal in another repetition period previous to said repetition period (see fig. 114).

As to claim 7, Tsuge teaches a driving circuit according to claim 1 (see above rejection), wherein the target voltage is a gray-scale voltage (see Abstract and [0001]).

As to claim 8, Tsuge teaches a driving circuit according to claim 1 (see above rejection), wherein the capacitive load is a liquid crystal cell (see [0022] and [0399]).

As to claim 9, Tsuge teaches a driving circuit according to claim 1 (see above rejection), wherein the driving signal supplying means includes analog to digital

converting means (note that it is well known in the art to use analog to digital or digital to analog converters in the signal drivers of LCD devices, see also fig. 10).

As to claim 10, Tsuge teaches a display device using a driving circuit according to claim 1 (see Abstract, [0001], and fig. 2).

4. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroshi Tsuchi (Pub. No.: US 2002/0021606).

As to claim 4, Tsuchi teaches a driving circuit for driving a capacitive load of a display device, comprising: driving signal supplying means for supplying a driving signal having a target voltage to be applied (see fig. 1 – driving circuit 1012); an amplifying stage for receiving the driving signal and selectively outputting the driving signal to the capacitive load (see figs. 6 & 7); a pair of power sources for selectively performing charging and discharging to the capacitive load, respectively (see fig. 8 – VDD and VSS); and comparing means having one input receiving a voltage value of the driving signal and the other input receiving a voltage value on an output line coupled to the capacitive load see fig. 8 – Vin, Vout, differential circuits 21 and 22 – note that it is obvious that the differential circuits are the same as the comparing means of applicants invention), the driving circuit repeating a repetitive operation including a pre-operation where charging or discharging is performed by any one of the power sources and then

stopped and a post-operation where the amplifying stage is switched to a state for outputting the driving signal to the capacitive load after the pre-operation (see figs. 11A and 11B and [0203]), the charging and discharging operation performed by the pair of the power sources being controlled based on a comparison output of the comparing means during the pre-operation (see figs. 7-10 and [0167]-[0170] – note that the charging means 30 and discharging means 40 are driven depending on the outputs of the differential amplifiers 21 and 22).

As to claim 5, Tsuchi teaches a driving circuit as defined in claim 4 (see above rejection), wherein a discharging operation is performed if the comparison output indicates that the voltage value on the output line is greater than the voltage value of the driving signal, an a charging operation is performed if the comparison output indicates that the voltage value on the output line is smaller than the voltage value of the driving signal (see [0165]-[0173]).

As to claim 6, Tsuchi teaches a driving circuit as defined in claim 5 (see above rejection), wherein one of the charging and discharging operations is continued until the comparison output indicates that the voltage value on the output line reaches the voltage value of the driving signal (see [0165]-[0173]).

Note: References cited include just some examples that Examiner feels best explain the prior art rejection. However, the entire references teach the scope of the claims in more detail. Examiner recommends that Applicant read the full disclosures.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Us Pub. Nos.: 2004/0008166 and 2006/0033697.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JENNIFER ZUBAJLO whose telephone number is (571)270-1551. The examiner can normally be reached on Monday-Friday, 8 am - 5 pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jennifer Zubajlo/
Examiner, Art Unit 2629
6/16/09

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629